

5. (Currently Amended) A transistor-type ferroelectric nonvolatile memory element according to claim 2, wherein the MIS structure is a MIS transistor of the nonvolatile memory element, and [[the]] regions of source and drain of the MIS transistor are separated by the trench.

6. (Previously Presented) A transistor-type ferroelectric nonvolatile memory element according to claim 1, wherein the MIS structure includes the rugged portion therein, the means for increasing the effective area is constituted by the rugged portion, the upper part of the MIS structure is flat, and the MFM structure is laminated thereon.

7. (Previously Presented) A transistor-type ferroelectric nonvolatile memory element according to claim 1, wherein the means for increasing the effective area is constituted by an MIM (metal-insulator-metal) structure provided between the MFM structure and the MIS structure.

8. (Original) A transistor-type ferroelectric nonvolatile memory element according to claims ~~2-6~~, wherein the effective area of a metal layer on the ferroelectric layer of the MFM structure is smaller than that of the ferroelectric layer.